AMENDMENTS TO THE CLAIMS

Claim 1 (Original): A non-volatile memory positioned on a substrate of a semiconductor wafer, the non-volatile memory comprising:

a main memory array region comprising:

at least one main memory cell, the main memory cell comprising a main source and a main drain positioned in the substrate of the semiconductor wafer;

at least one main bit line, the main bit line being electrically connected to the main drain of the main memory cell; and

at least one main ground line, the main ground line being electrically connected to the main source of the main memory cell;

a redundant memory array region connected to the main memory array region, the redundant memory array region comprising:

at least one redundant memory cell, the redundant memory cell comprising a redundant source and a redundant drain positioned in the substrate of the semiconductor wafer;

at least one redundant bit line, the redundant bit line being electrically connected to the redundant drain of the redundant memory cell; and

at least one redundant ground line, the redundant ground line being electrically connected to the redundant source of the redundant memory cell; and

a common source used as the main source and the redundant source formed between the main memory array region and the redundant memory array region.

Claim 2 (Original): The non-volatile memory of claim 1 further comprising a peripheral circuit region having:

a main memory ground line decoder electrically connected to the main ground lines in the main memory array region;

a redundant memory ground line decoder electrically connected to the redundant ground lines in the redundant memory array region; and

at least two signal pass lines, two ends of each of the signal pass lines being electrically connected to the main memory ground line decoder and the redundant memory ground line decoder, respectively.

Claim 3 (Original): The non-volatile memory of claim 2 wherein the common source is electrically connected to a common ground line, and when the main memory ground line decoder addresses the common ground line, the main memory ground line decoder passes a signal to the redundant memory ground line decoder through the signal pass line to determine a potential of the common ground line and to generate an open-circuit between the common ground line and the redundant memory ground line decoder, and when the redundant memory ground line decoder addresses the common ground line, the redundant memory ground line decoder passes a signal to the main memory ground line decoder through the other signal pass line to determine a potential of the common ground line and to generate an open-circuit between the common ground line and the main memory ground line decoder.

Claim 4 (Original): The non-volatile memory of claim 3 wherein a sub-decoder of the main memory ground line decoder is electrically connected to the common ground line and

comprises a three-input NAND gate having three inputs for receiving an address signal, a first inverter having a first input electrically connected to an output of the three-input NAND gate, and a first tri-state inverter having a control end electrically connected to an output of a four-input NAND gate, the four-input NAND gate having four inputs and being formed in a sub-decoder of the redundant memory ground line decoder for receiving an address signal and a corresponding signal, the sub-decoder of the redundant memory ground line decoder being electrically connected to the common ground line and further comprising a second inverter and a second tri-state inverter, an input of the second inverter being electrically connected to an output of the four-input NAND gate, a control end of the second tri-state inverter being electrically connected to an output of the three-input NAND gate.

Claim 5 (Original): The non-volatile memory of claim 2 wherein the common source is electrically connected to a common ground line, and when the main memory ground line decoder addresses the common ground line, the main memory ground line decoder passes a signal to the redundant memory ground line decoder through the signal pass line so as to select the sub-decoders connected to the common ground line and cause the selected sub-decoders to generate an equal-potential output, and when the redundant memory ground line decoder addresses the common ground line, the redundant memory ground line decoder passes a signal to the main memory ground line decoder through the signal pass line to select the sub-decoders electrically connected to the common ground line and generate an equal-potential output.

Claim 6 (Original): The non-volatile memory of claim 5

wherein a sub-decoder of the main memory ground line decoder is electrically connected to the common ground line and comprises a three-input NAND gate having three inputs for receiving an address signal, a first NAND gate having an input electrically connected to an output of the three-input NAND gate and the other input electrically connected to an output of a four-input NAND gate, and a first inverter, the four-input NAND gate having four inputs and being formed in a sub-decoder of the redundant memory ground line decoder for receiving an address signal and a corresponding signal, the sub-decoder of the redundant memory ground line decoder being electrically connected to the common ground line and further comprising a second two-input NAND gate and a second inverter, an input of the second two-input NAND gate being electrically connected to an output of the four-input NAND gate, the other input of the second two-input NAND gate being electrically connected to an output of the three-input NAND gate in a sub-decoder of the main memory ground line decoder.

Claim 7 (Original): The non-volatile memory of claim 1 wherein the non-volatile memory has a virtual ground array structure.

Claim 8 (Original): A non-volatile memory positioned on a substrate of a semiconductor wafer, the non-volatile memory comprising:

a main memory array region comprising:

at least one main memory cell, the main memory cell comprising a main source and a main drain positioned in the substrate of the semiconductor wafer;

at least one main bit line, the main bit line being electrically connected to the main drain of the main

memory cell; and

at least one main ground line, the main ground line being electrically connected to the main source of the main memory cell;

a redundant memory array region connected to the main memory array region, the redundant memory array region comprising:

at least one redundant memory cell, the redundant memory cell comprising a redundant source and a redundant drain positioned in the substrate of the semiconductor wafer;

at least one redundant bit line, the redundant bit line being electrically connected to the redundant drain of the redundant memory cell; and

at least one redundant ground line, the redundant ground line being electrically connected to the redundant source of the redundant memory cell; and

a common drain used as the main drain and the redundant drain formed between the main memory array region and the redundant memory array region.

Claim 9 (Original): The non-volatile memory of claim 8 further comprising a peripheral circuit region having:

a main memory bit line decoder electrically connected to the main bit lines in the main memory array region;

a redundant memory bit line decoder electrically connected to the redundant bit lines in the redundant memory array region; and

at least two signal pass lines, two ends of each of the signal pass lines being electrically connected to the main memory bit line decoder and the redundant memory bit line decoder, respectively.

Claim 10 (Original): The non-volatile memory of claim 9 wherein the common drain is electrically connected to a common bit line, and when the main memory bit line decoder addresses the common bit line, the main memory bit line decoder passes a signal to the redundant memory bit line decoder through the signal pass line to determine a potential of the common bit line and to generate an open-circuit between the common bit line and the redundant memory bit line decoder, and when the redundant memory bit line decoder addresses the common bit line, the redundant memory bit line decoder passes a signal to the main memory bit line decoder through the other signal pass line to determine a potential of the common bit line and to generate an open-circuit between the common bit line and the main memory bit line decoder.

Claim 11 (Original): The non-volatile memory of claim 10 wherein a sub-decoder of the main memory bit line decoder is electrically connected to the common bit line and comprises a three-input NAND gate having three inputs for receiving an address signal, a first inverter having an input electrically connected to an output of the three-input NAND gate, and a first tri-state inverter having a control end electrically connected to an output of a four-input NAND gate, the four-input NAND gate having four inputs and being formed in a sub-decoder of the redundant memory bit line decoder for receiving an address signal and a corresponding signal, the sub-decoder of the redundant memory bit line decoder being electrically connected to the common bit line and further comprising a second inverter and a second tri-state inverter, an input of the second inverter being electrically connected to an output of the four-input NAND gate, an input of the second

tri-state inverter being electrically connected to an output of the three-input NAND gate in a sub-decoder of the main memory bit line decoder.

Claim 12 (Original): The non-volatile memory of claim 9 wherein the common drain is electrically connected to a common bit line, and when the main memory bit line decoder addresses the common bit line, the main memory bit line decoder passes a signal to the redundant memory bit line decoder through the signal pass line so as to select the sub-decoders electrically connected to the common bit line and generate an equal-potential output, and when the redundant memory bit line decoder addresses the common bit line, the redundant memory bit line decoder passes a signal to the main memory bit line decoder through the signal pass line to select the sub-decoders electrically connected to the common bit line and generate an equal-potential output.

Claim 13 (Original): The non-volatile memory of claim 12 wherein the sub-decoder of the main memory bit line decoder is electrically connected to the common bit line and comprises a three-input NAND gate having three inputs for receiving an address signal, a first NAND gate having an input electrically connected to an output of the three-input NAND gate and the other input electrically connected to an output of a four-input NAND gate, and a first inverter, the four-input NAND gate having four inputs and being formed in a sub-decoder of the redundant memory bit line decoder for receiving an address signal and a corresponding signal, the sub-decoder of the redundant memory bit line decoder being electrically connected to the common bit line and further comprising a second two-input NAND gate and a second inverter, an input

of the second two-input NAND gate being electrically connected to an output of the four-input NAND gate, the other input of the second two-input NAND gate being electrically connected to an output of the three-input NAND gate in a sub-decoder of the main memory bit line decoder.

Claim 14 (Original): The non-volatile memory of claim 8 wherein the non-volatile memory has a virtual ground array structure.

Claims 15-25 (canceled)

Claim 26 (Original): A non-volatile memory positioned on a substrate of a semiconductor wafer, the non-volatile memory comprising:

a main memory array region comprising:

at least one main memory cell, the main memory cell comprising a main source and a main drain positioned in the substrate of the semiconductor wafer;

at least one main bit line, the main bit line being electrically connected to the main drain of the main memory cell; and

at least one main ground line, the main ground line being electrically connected to the main source of the main memory cell;

a redundant memory array region connected to the main memory array region, the redundant memory array region comprising:

at least one redundant memory cell, the redundant memory cell comprising a redundant source and a redundant drain positioned in the substrate of the semiconductor wafer;

at least one redundant bit line, the redundant bit line being electrically connected to the redundant drain of the redundant memory cell; and

at least one redundant ground line, the redundant ground line being electrically connected to the redundant source of the redundant memory cell, wherein a common doped region is commonly used by the main memory array region and the redundant memory array region; and

a peripheral circuit region comprising at least one decoder.

Claim 27 (Original): The non-volatile memory of claim 26 wherein the decoder comprises:

a main memory ground line decoder electrically connected to the main ground lines in the main memory array region;

a redundant memory ground line decoder electrically connected to the redundant ground lines in the redundant memory array region; and

at least two signal pass lines, two ends of each of the signal pass lines being electrically connected to the main memory ground line decoder and the redundant memory ground line decoder, respectively.

Claim 28 (Original): The non-volatile memory of claim 27 wherein the decoder further comprises a common ground line decoder.

Claim 29 (Original): The non-volatile memory of claim 26 wherein the common doped region is used as the main source and the redundant source formed between the main memory array region and the redundant memory array region.

Claim 30 (Original): The non-volatile memory of claim 26 wherein the decoder comprises:

a main memory bit line decoder electrically connected to the main bit lines in the main memory array region;

a redundant memory bit line decoder electrically connected to the redundant bit lines in the redundant memory array region; and

at least two signal pass lines, two ends of each of the signal pass lines being electrically connected to the main memory bit line decoder and the redundant memory bit line decoder, respectively.

Claim 31 (Original): The non-volatile memory of claim 30 wherein the decoder further comprises a common bit line decoder.

Claim 32 (Original): The non-volatile memory of claim 26 wherein the common doped region is used as the main drain and the redundant drain formed between the main memory array region and the redundant memory array region.